

1        1. A system wherein data is read from, and store in, a memory, such data having  
2        associated therewith an address/control portion, such system comprising:

3              (A) a pair of controller sections, one of such sections being a primary section and the  
4        other one of the sections being a secondary section, both such sections being configured to  
5        implement identical control logic in controlling the transfer of such data between a first port  
6        connected to the pair of control sections and a write data port, the write data port of the  
7        primary section being connected to the memory, such first port receiving an address/control  
8        portion associated with the data; and

9              (B) a checker producing a NOOP command to the memory if logic signal produced  
10      by the pair of control logic from the address/control portion at the first port are different from  
11      one another.

1        2. The system recited in claim 1 wherein the memory is configured to inhibit storage  
2        of data in the memory at the data port in response to the NOOP command.

1        3. A system wherein data is read from, and store in, a memory, such data having  
2        associated therewith an address/control portion, such system comprising:

3              (A) a pair of controller sections, one of such sections being a primary section and the  
4        other one of the sections being a secondary section, both such sections being configured to  
5        implement identical control logic in controlling the transfer of such data between a first port  
6        connected to the pair of control sections and a write data port of the primary section, the  
7        write data port of the primary section being connected to the memory, such first port  
8        receiving the address/control portion associated with the data; and

9              (B) a checker producing a NOOP command to the memory if a parity bit generated by  
10      a first parity generator in the primary section from the address/control portion at the first port  
11      and a parity bit generated by the first parity generator of the secondary section from the  
12      address/control portion at the first port are the same, or different.

1        4. The system recited in claim 3 wherein the memory is configured to inhibit storage  
2        of data at the data port in the memory in response to the NOOP command.

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5. A system wherein data is read from, and store in, a memory, such data having  
2 associated therewith an address/control portion, such system comprising:

3 (A) a pair of controller sections, one of such sections being a primary section and the  
4 other one of the sections being a secondary section, both such sections being configured to  
5 implement identical control logic in controlling the transfer of such data between a first port  
6 connected to the pair of control sections and a write data port of the primary section, such  
7 write data port of the primary section being connected to the memory, such first port  
8 receiving the address/control portion associated with the data; and

9 (B) a checker producing a NOOP command to the memory if the digital word  
10 generated by a first parity generator of primary section from the address/control portion at the  
11 first port and the digital word generated by a first parity generator of secondary section from  
12 the address/control portion at the first port are the same or different.

1 6. The system recited in claim 5 wherein the memory is configured to inhibit storage  
2 of data at the data port in the memory in response to the NOOP command.

1 7. A system wherein data is read from, and store in, a memory, such data having  
2 associated therewith an address/control portion, such system comprising:

3 (A) a pair of controller sections, one of such sections being a primary section and the  
4 other one of the sections being a secondary section, both such sections being configured to  
5 implement identical control logic in controlling the transfer such data between a first port  
6 connected to the pair of control sections and a write data port of the primary section, such  
7 write data port of the primary section being connected to the memory, such first port  
8 receiving the address/control portion associated with the data; and

9 (B) a checker producing a NOOP command to the memory if a parity bit generated by  
10 a first parity generator in the primary section the address/control portion at the first port and a  
11 parity bit generated by the first parity generator of the secondary section from the  
12 address/control portion at the first port are the same, or different, or if a digital word  
13 generated by the first parity generator of primary section a digital word generated by the first  
14 parity generator of secondary section from the address/control portion at the port are the  
15 same or different.

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8. The system recited in claim 7 wherein the memory is configured to inhibit storage  
2 of data in the memory at the data port in response to the NOOP command.

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2 9. A system wherein data is read from, and stored in, a memory, such data having  
associated therewith an address/control portion, such system comprising:

3 (A) a pair of controller sections, one of such sections being a primary section  
4 and the other one of the sections being a secondary section, both such sections being  
5 connected to a first port, both such sections being configured to implement identical  
6 control logic in controlling the transfer of such data between the first port and the write  
7 data port, each one of the sections, comprising:

8 a first parity generator coupled to the first port; for generating a parity  
9 bit for an address/control digital word, such digital word comprising  
10 the address/control portion associated with the data at such first port;

11 (B) a checker, comprising:

12 a second parity generator for generating a parity bit from the digital  
13 word and for passing there-through to an address/control port either:

14 the parity bit generated by the second parity generator or,  
15 an inverted parity bit of the parity bit generated by the second  
16 parity bit generator, selectively in accordance with:

17 whether the parity bit generated by the first parity generator in  
18 the primary section and the parity bit generated by the first parity  
19 generator of the secondary section are the same, or different, or if the  
20 digital word generated by the first parity generator of primary section  
21 and the digital word generated by the first parity generator of  
22 secondary section are the same or different.

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2 10. The system recited in claim 9 wherein the memory is configured to inhibit  
storage of data at the data port in the memory if either:

3 the inverted parity bit of the inverter is passed through the selector to the  
4 address/control port because either the parity bit generated by the first parity  
5 generator in the primary section and the parity bit generated by the first parity  
6 generator of the secondary section are different; or

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the digital word generated by the first parity generator of primary section and  
the digital word generated by the first parity generator of secondary section are  
different.

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1        11. A system wherein data is read from, and store in, a memory, such data having  
2        associated therewith an address/control portion, such system comprising:

3        a controller having:

4            (A) a first port:

5                  for receiving data to be stored in the memory; and

6                  for receiving the address/control portion associated with such data;

7            (B) an address/control port connected to the memory for transmitting address  
8        and memory read/write control signals to the memory;

9            (C) a write data port connected to the memory for transmitting data to be  
10      stored in the memory;

11        (D) a pair of controller sections, one of such sections being a primary section  
12      and the other one of the sections being a secondary section, both such sections being  
13      connected to the first port, both such sections being configured to implement identical  
14      control logic in controlling the transfer such data between the first port and the write  
15      data port, each one of the sections, comprising:

16                  a first parity generator coupled to the first port; for generating a parity  
17      bit for an address/control digital word, such digital word comprising  
18      the address/control portion associated with the data at such first port;

19            (E) a checker, comprising:

20                  a second parity generator for generating a parity bit from the digital  
21      word and for passing there-through to an address/control port either:

22                          the parity bit generated by the second parity checker; or,  
23                          the inverted parity bit of the inverter, selectively in accordance  
24      with:

25                  whether the parity bit generated by the first parity generator in  
26      the primary section and the parity bit generated by the first parity  
27      generator of the secondary section are the same, or different, or if the  
28      digital word generated by the first parity generator of primary section

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and the digital word generated by the first parity generator of  
secondary section are the same or different.

1           12. The system recited in claim 11 wherein the memory is configured to inhibit  
2           storage of data at the data port in the memory if either:

3                 the inverted parity bit of the inverter is passed through the selector to the  
4                 address/control port because either the parity bit generated by the first parity  
5                 generator in the primary section and the parity bit generated by the first parity  
6                 generator of the secondary section are different; or

7                 the digital word generated by the first parity generator of primary section and  
8                 the digital word generated by the first parity generator of secondary section are  
9                 different.

10           13. A system wherein data is read from, and stored in, a memory, such data having  
11           associated therewith an address/control portion, such system comprising:

12                 a controller having:

13                 (A) a first port:

14                         for receiving data to be stored in the memory and for transmitting data  
15                         read from the memory; and

16                         for receiving the address/control portion associated with such data;

17                 (B) an address/control port connected to the memory for transmitting address  
18                 and memory read/write control signals to the memory to the controller;

19                 (C) a read data port connected to the memory for receiving data read from the  
20                 memory;

21                 (D) a write data port connected to the memory for transmitting data to be  
22                 stored in the memory;

23                 (E) a pair of controller sections, one of such sections being a primary section  
24                 and the other one of the sections being a secondary section, both such sections being  
25                 connected to the first port, both such sections being configured to implement identical  
26                 control logic in controlling the transfer such data between the first port and the read  
27                 and write data ports, each one of the sections, comprising:

a first parity generator coupled to the first port; for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port;

(F) a checker, comprising:

(a) a second parity generator for generating a parity bit for the address/control digital word generated by the primary section;

(b) an inverter for inverting the parity bit generated by the second parity bit generator;

(c) a selector for passing there-through to the address/control port  
either:

the parity bit generated by the second parity checker; or,

the inverted parity bit of the inverter, selectively in accordance

with:

whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are the same or different.

14. The system recited in claim 13 wherein the memory is configured to inhibit storage of data at the data port in the memory if either:

the inverted parity bit of the inverter is passed through the selector to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or

the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are different.